Scientific, Back-Illuminated CCD Development for the Transiting Exoplanet Survey Satellite

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***Abstract*— We describe the development of the fully depleted, back illuminated charge coupled devices for the Transiting Exoplanet Survey Satellite, which includes a set of four wide angle telescopes, each having a 2x2 array of CCDs. The devices are fabricated on the newly upgraded 200-mm wafer line at Lincoln Laboratory. We discuss methods used to produce the devices and present early performance results from the 100-micron thick, 15x15-µm, 2k x 4k pixel frame transfer CCDs.**

Keywords: CCD, TESS, deep depletion, quantum efficiency

I. Introduction

The mission of NASA's Transiting Exoplanet Survey Satellite, or TESS, is to detect earth-size exoplanets during a two-year, all sky survey [1]. TESS will monitor hundreds of thousands of stars that are bright enough for follow up measurements from ground- and space-based observatories. Exoplanets are detected by measuring the dip in the apparent brightness of a star from a transiting planet. Identification of small planets requires high photometric precision and the spectral type of the target stars requires detectors with sensitivity out to 1000nm. Besides detection of transiting planets, TESS will be used to measure planet characteristics such as diameter, mass, surface gravity, and temperature. The superb spatial uniformity, sensitivity, and other performance attributes of charge-coupled devices suit them superbly for this application. The TESS payload consists of four identical cameras, each having a four-CCD mosaic in its focal plane. Figure 1 shows a picture of a prototype 2x2 CCD assembly with frame-store light shield cover removed.

Over the past decades Lincoln Laboratory has advanced development of its CCD technology to address new performance needs in scientific applications [2] [3]. Beginning in early 2011, the Lincoln Laboratory Microelectronics Laboratory moved from 150-mm-wafer based to 200-mm-wafer based device fabrication. The 200-mm-wafer semiconductor process tools offer better feature definition and uniformity than the older 150-mm toolset, and deliver improved capability for large-format CCD and CMOS image sensors. Instead of the earlier 150-mm full-wafer scanner lithography method, newer imagers design are fabricated on 200-mm silicon substrates using an i-line photolithography stepper. The facility supports complete fabrication starting from preparation of high-resistivity float zone silicon substrates through back illumination.

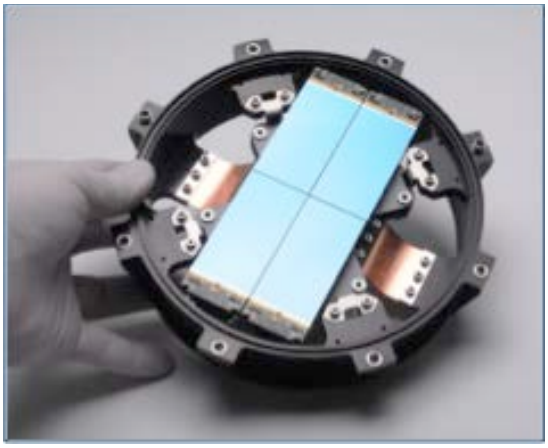

Fig. 1. The detector assembly of one of the prototype lenses. The light shield cover for the frame store regions is removed.

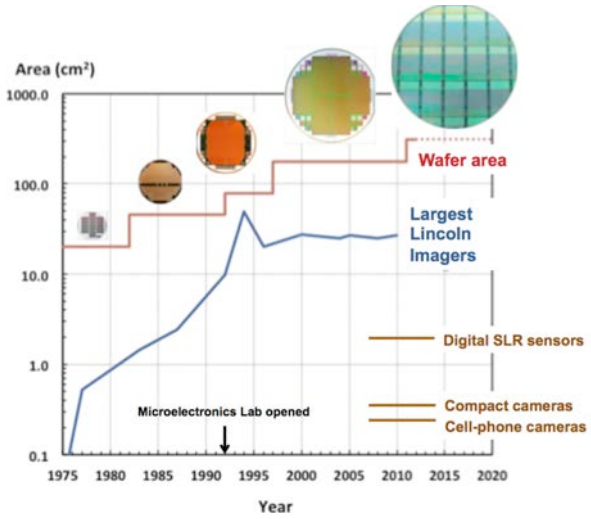

Fig. 2. Wafer size progression at MIT-LL's Microelectronics Laboratory.

The specifications for TESS required thick (100µm) fully depleted CCDs with 2048x2048 imaging array and 2048x2048 frame store regions, with 15x15µm pixels. Rapid (~4msec) frame transfer and high (> 200,000 electrons) well capacity are required.

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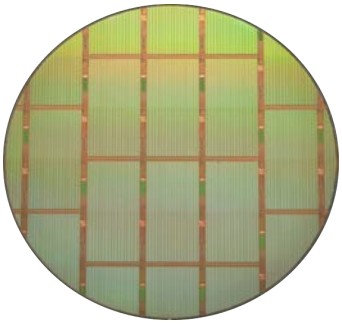

Fig. 3. Photograph of a completed front-illuminated, 200-mm diameter wafer including eight CCID-80 imagers. The device pattern is stepped across the wafer with partial die to aid back-end film planarization.

II. CCID-80 Device Description

The CCID80, developed for TESS, is a deep-depletion, frame-transfer CCD with a full frame store. The device has four outputs; each output is associated with an array of 512(H) x 2048(V) imaging pixels, for a total imaging area of 2048(H) x 2048(V). The die size is 32(W) x 64(H) mm for an area of 20.4 cm^2.

The imaging array, frame store, and serial registers all consist of conventional three-phase, 15x15 µm pixels. There is a three-phase charge injection register at the top of the array, and the serial register support bidirectional transfer. The pixel array employs a trough design feature to provide radiation mitigation for small charge packets. To enable the desired fast frame transfer time, the image array and frame store clocks are strapped with metal interconnect to reduce the RC delay from the clock lines. The output circuit is a single-stage MOSFET similar to others demonstrated at Lincoln Laboratory.

III. Front Illuminated CCD Fabrication and Test

The starting material for this work was 200-mm diameter, <100>, float zone refined p-type silicon with resistivity greater than 5000 ohm-cm. With the exception of photolithography, the fabrication steps are quite similar to those practiced on 150-mm diameter wafers, however new tools and recipes were required to replicate or improve upon the fabrication steps.

It is a three-polysilicon, two-metal process technology requiring fourteen lithography levels to complete the device to front-illumination testing. Figure 3 shows a photograph of a completed front illumination wafer. The narrow vertical metal traces for parallel clock strapping can also be seen in this photograph.

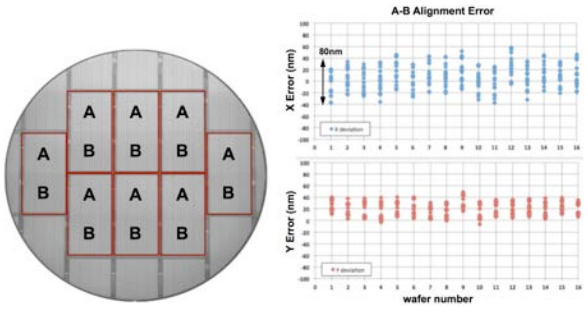

Fig. 4. Each CCD is stitched to connect the image array (A) and frame store (B), as shown to the left. The data to the right shows X and Y alignment error between A-B fields. We achieve approximately 80-nm or better alignment error between fields in both directions across a sixteen wafer lot. This is well within the design requirements for a 15-µm pixel.

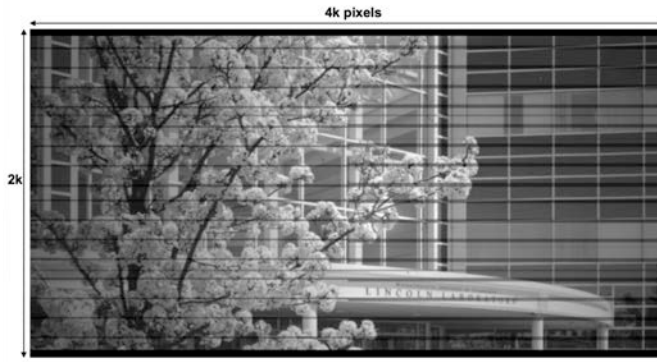

Fig. 5. Raw front illumination device imagery captured by projecting a slide onto the device at 0°C with 1 second integration time. The metal straps for clock lines are seen to obstruct the image.

A wide field (5x5 cm) Canon IW stepper is used for all lithography levels. However, since the CCD's physical dimension exceeds this exposure field, we exploit die stitching to photocompose the image array and frame store sections on the wafer. This approach is illustrated in Figure 4 with exposure field "A" representing the Image Array and "B" representing the Frame Store. We consistently achieve less than 100-nm of stitch error between these fields (the data shows 80-nm or better overlay error across a 16 wafer lot). For a three-phase, 15-µm pixel, this amounts to less than one percent of a CCD phase.

After front illumination fabrication, each device is tested with an automatic wafer prober to assess functionality. We perform imaging tests by projecting an emulsion slide onto the chip surface. Figure 5 shows raw imagery captured by CCID80 at 0°C with 1 second integration time.

IV. Back Illuminated CCD Performance

Lincoln Laboratory supports several different styles of back illuminated processing. For TESS, we use a flow that involves: epoxy mounting the device wafer to a support wafer; wet chemical thinning the high resistivity float zone silicon to the 100-micron full depletion target; back-side passivation through an ion implantation, laser annealing sequence; deposition and patterning of anti-reflection and light shield coatings; and etches to provide access to the bond pads.

Figure 6 shows a photograph of a completed back illumination wafer. The frame store regions of each CCD are covered with a thin aluminum layer. We again perform imaging tests by projecting an emulsion slide onto the chip

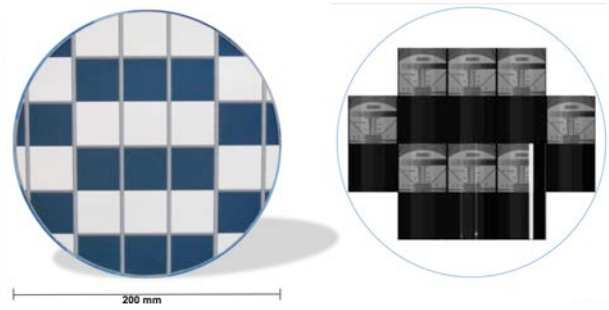

Fig. 6. At the left is a photograph of a completed back-illuminated, 200-mm diameter wafer; the frame store regions are now covered with an integrated aluminum light shield. At the right is a composition of test data arranged as a wafer map. The imagery is captured at a wafer probe test at +20°C with 1 second integration time.

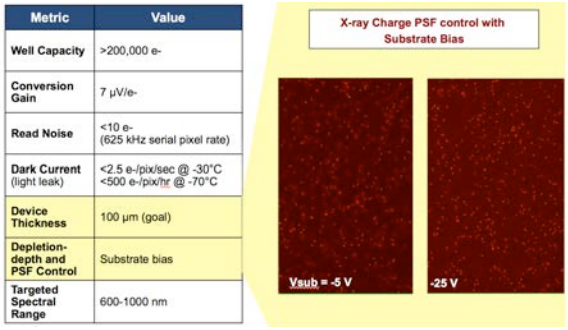

Fig. 7. Summary of wafer level testing for typical back illuminated CCID-80 devices. An ^{55}Fe source is used to generate the xray events.

surface; this figure also shows the results for all die tested arranged as they are positioned on a wafer.

It is noteworthy that this imagery was captured in full-field integration mode at +20°C with a 1 sec integration time. The device dark current is low enough to permit reasonable contrast in room temperature operation from this large-area, 100-micron thick silicon device. The defects on this wafer include a gate to substrate short on the lower, right-most device. Overall port yield has been very high, with only one failed port out of a lot of 16 wafers (512 ports).

Figure 7 summarizes the initial performance metrics for this device. At this point, test system constraints such as stray light and noise limit the accuracy of our measurements. The right side of Figure 7 illustrates the change in x-ray induced charge point spread function with substrate bias. The charge clouds become more focused to single pixel events with the application of -25V substrate bias. A histogram of these events is used to estimate the device charge conversion gain.

The true benefit of the 100-micron thick detector is shown in the Figure 8 spectral response curve. We observe over 20% improvement in quantum efficiency at 1000nm measurement wavelength over a 45-micron thick device.

V. Summary

We have described the detectors developed for the Transiting Exoplanet Survey Satellite. A total of sixteen

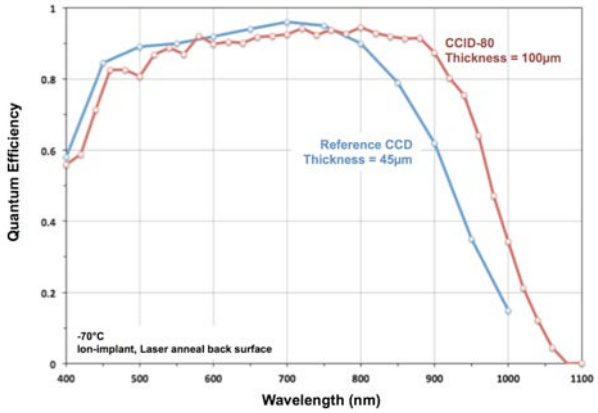

Fig. 7. Summary of wafer level testing for typical back illuminated CCID-80 devices.

devices arranged in four mosaics will be needed. Initial performance results were discussed.

Acknowledgment

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